REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested. Claim amendments are presented herein to obviate the current rejection. No new matter has been added.

35 USC § 112

Claim 7 has been amended to recite "the defined signal parameter".

It is respectfully submitted that claim 15, line 6 was previously amended to recite a "central database" (although it may have been difficult to visually recognize such amendment).

Accordingly, it is respectfully requested that the rejections under 35 USC § 112 be withdrawn.

35 USC § 103

Claims 1, 3-7, 9-18, and 20-25 stand rejected under 35 USC § 103 based on various combinations of ExpressiveSystems, IEEEVerilog, and Yamagishi. These rejections are respectfully traversed.

Claim 1 has been amended to recite: "wherein the automatically updating comprises modifying the logic design to

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be compatible with the modified signal parameters". Similar amendments were made to claims 7, 15, and 18.

ExpressiveSystems describes an arrangement in which "Double clicking the signal editor allowing detailed changes to be made and applied to the local level or the entire design" (see, ExpressiveSystems p. 8). The office action interprets this passage to disclose "wherein the logic design module is operable to automatically update the logic design when the signal parameters in the central database are modified" in claim 1 as well as similar features in the other independent claims. However, it is respectfully submitted that ExpressiveSystems does not unambiguously or even impliedly describe or suggest the subject matter recited in the claims. In order to further clarify this difference, the claims have been amended to recite that the logic design is modified so that it is compatible with the modified signals. The cited passage in Expressive Systems does not suggest that there is any modification to a logic design in response to a change of a signal in the signal editor. Rather, Expressive Systems simply states that changes may be applied to an entire design. This statement simply does not disclose the subject matter recited in the claims.

Moreover, Yamagishi fails to describe or even suggest a central database in which modifiable signal parameters are available to user nor a central database integrated into a logic

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design module. Rather, Yamagishi describes an arrangement in which design data is stored in a database to allow for incremental compiling (see, inter alia, Yamagishi section 2.3). There is no suggestion that this database stores data relating to signal parameters that may be modified by a plurality of users. Therefore, the skilled artisan would not have been motivated to combine ExpressiveSystems with Yamagishi nor would a skilled artisan have combined these two references to result in the recited subject matter without an unreasonable expectation of success.

Furthermore, with regard to claims 3, 20, and their dependent claims, the references fails to disclose or otherwise suggest a logic design module that is structured and arranged to indicate design discrepancies automatically in the logic design resulting from the modifications to the signal parameters in the central database. IEEEVerilog describes an arrangement in which an error occurs if there are to many or too few bits to connect to all instances. In other words, IEEEVerilog relates to an arrangement in which factors such as a number of bits are used to determine whether certain instances may be connected. This reference does not suggest that discrepancies in previously connected instances are automatically detected when a parameter is changed. Moreover, IEEEVerilog does not suggest that any discrepancies are indicated to a user. Therefore, the skilled

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artisan would not have combined ExpressiveSystems, Yamagishi, and IEEEVerilog to result in the subject matter of claims 3, 20, and their respective dependent claims.

Accordingly, the claims should be allowable.

Concluding Comments

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

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Applicant asks that all claims be allowed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 12-30-05

Scott C. Harris
Reg. No. 32,030
Attorney for Intel Corporation

Fish & Richardson P.C.
12390 El Camino Real
San Diego, California 92130
(858) 678-5070 telephone
(858) 678-5099 facsimile

CARL A. K[illegible]NEN, III
REG. NO. 42,773

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